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Frank Vahid Professor, Programming Embedded Systems, Digital Design, Java. See zybooks.com; Book: Digital Design + VHDL/Verilog books (Wiley 2006, 2011)

Register-transfer level - wikipedia, the free

register-transfer level (RTL) is a design abstraction like Verilog and VHDL to Design at the RTL level is typical practice in modern digital design

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